This tutorial is intended as a supplementary learning tool for students of Com S 321, an undergraduate course on computer architecture taught at Iowa State University. The textbook for the course is "Computer Organization and Design: The Hardware/Software Interface" by Hennessy and Patterson. The concepts explained include some aspects of computer performance, cache design, and pipelining. Examples, interactive applets, and some problems with solutions are used to illustrate basic ideas. Most of the material has been developed from the textbook as well as from "Computer Architecture: A Quantitative Approach" by the same authors. The problems that have been solved have been taken from a number of sources, but the solutions are unique in the sense that emphasis has been placed not only on the answers but also on the reasoning processes that will help students solve similar problems.

To be able to see and interact with java applets in this tutorial, please enable Java in your browser. If you work with Netscape browser, go to Edit/Preferences/Advanced and check the box "Enable Java".

Feedback consisting of comments and errors are welcome, and can be e-mailed
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Topics

✗ Computer Performance
  • Amdahl's Law
  • Computer Performance - I
  • Computer Performance - II

✗ Memory Hierarchy Design
  • Principles and Levels
  • Make the Common Case Fast
    • Amdahl's Law
  • Principle of Locality
  • Smaller is Faster
  • Common Questions
    • Block Placement
      • Placement Methods
      • Examples
    • Block Identification
      • Address Structure
      • Examples
    • Block Replacement
      • Policies
      • Interactive applet to check different policies
        • Example (a problem)
    • Interaction with Memory
      • On Read
      • On Write
      • Interactive Diagram
        • Example (a problem)

✗ Pipelining
  • Classification of Instruction Sets
  • Addressing Modes
    • Memory Interpretation
    • Memory Alignment
  • DLX architecture
    • Instruction Set
    • Instruction Layout
    • Examples of Instructions
    • An Implementation of DLX
    • The Basic Pipeline for DLX
Performance Issues in Pipelining

Pipeline Hazards
  Performance in Pipeline with Stalls
  Structural Hazards
  Data Hazards
    Forwarding
    Data Hazard Classification
    When Stalls are Required
    Pipeline Scheduling
  Control Hazards
    Branch Prediction Schemes
      Predict Not Taken
      Delayed Branch
      Cancelling Branch
    Problem on Branch Prediction Schemes
  Problem on Pipeline Hazards

Dealing with Exceptions
  Types of Exceptions
  Exceptions in DLX

Pipeline with Multicycle Operations

Instruction Level Parallelism
  Loop Unrolling
  Dynamic Scheduling Techniques